ABSTRACT

DESIGN AND IMPLEMENTATION OF UART USING VHDL

Objective of the project:

1. Study of Serial UART

2. Behavioral/RTL modeling of Design blocks

3. Design of stimulus modules to test the functionality of Design.

4. Synthesize design to extract Gate level net list.

Description

This UART (Universal Asynchronous Receiver Transmitter) is designed to make an interface between a RS232 line and a microcontroller, or an IP core.

It works fine connected to the serial port of a PC for data exchange with custom electronic.

It integrates two separate clocks, one for wishbone bus, and the other for bit stream generation. This has the advantage to let the user bring his own desired frequency for the baud rate.

Baud rate divisor from 1 to 65536 (generic parameter set at integration time)

Does not support: FIFO input/output, Control handshaking

This Design coding, Simulation, Logic Synthesis and Implemented will be done using various EDA tools.

Block Diagram of UART